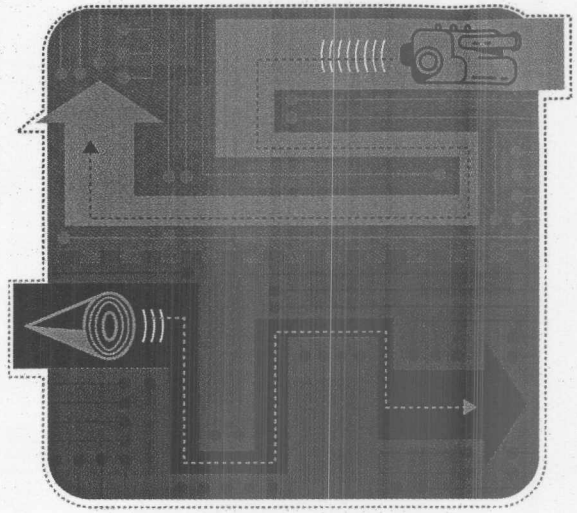

IEEE 1149 EXPANDS DIFFERENTIALLY

THE VENERABLE STANDARD ADDS SUPPORT FOR THE DIFFERENTIAL SIGNALS FOUND IN SERIAL BUSES.

BRIAN STEARNS, NATIONAL SEMICONDUCTOR

Serial buses, which provide the bandwidth needed to bring streaming audio and video to computers and communications systems, are replacing the parallel buses that typically traverse cables and backplanes. To achieve the bandwidth necessary to keep the data bits flowing quickly, serial buses use AC-coupled, differential signals, a technique that complicates the testing challenge.

The IEEE 1149.1 boundary-scan (JTAG) standard was sufficient for testing parallel, single-ended networks, but it is useless for testing AC-coupled differential networks. The IEEE has addressed this limitation with IEEE 1149.6, which extends the boundary-scan standard to handle the signaling in today's serial buses (Ref. 1).

Serial vs. parallel

Parallel, TTL-level buses have widened to 64 bits, but their low bandwidth (tens of megahertz) limits their usefulness. Physical space and switching noise prevent parallel buses from keeping up with bandwidth demand.

PCI Express, Fibre Channel, Serial ATA, and other serial buses consume far less physical space than their parallel cousins. They use serializer/deserializer (SerDes) devices to serialize multiple channels of parallel TTL-level signals into a single high-speed data stream. At the receiver, another SerDes device deserializes the serial stream back to TTL-level (single-ended signaling) channels (**Figure 1**).

For an 8-bit TTL bus that operates at 66 MHz, a SerDes device can convert the bus to a serial stream operating at a 528-MHz data rate. In reality, the bus will need as much as 1 GHz of bandwidth to cover the overhead associated with sending the data in packets. In a serial configuration, the number of conductors drops from eight to two, which reduces signal noise and saves board space. Many IC manufacturers provide a variety of SerDes functions using an assortment of technologies, including low-voltage differential signaling (LVDS), current-mode logic (CML), and low-voltage positive emitter-coupled logic (LVPECL).

To eliminate threshold offsets, engineers AC-couple serial signals by inserting capacitors into the high-speed interconnects between drivers and receivers. AC-coupling also eliminates ground offsets if the driver and receiver are on different cards or use different power supplies. The capacitors act as a high-pass filter, eliminating the DC bias of the signal while passing the high-speed signals. To further maintain DC balance in the data stream, most high-speed SerDes devices use an 8b/10b encoding scheme, which keeps the number of 1's and 0's roughly equal.

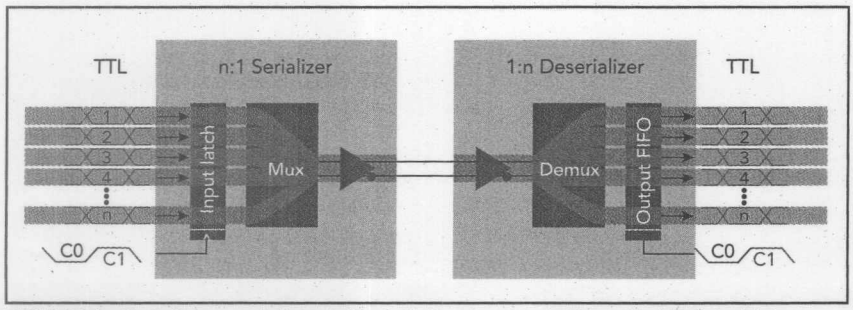

FIGURE 1. Serializers and deserializers help migrate single-ended TTL to high-speed differential signals.

Test issues

With single-ended TTL buses, you can use IEEE 1149.1 to verify the connections. As long as a system contains JTAG-enabled drivers and receivers, you can sufficiently check the integrity of these single-ended connections using basic JTAG techniques.

The IEEE 1149.1 standard, however, was never intended for differential networks. It falls short in environments that contain frequency-dependent parasitic components. At the higher data rates of the differential environment, the conductors behave like a transmission line, and you must include all the frequency-dependent parasitic components in any model of the serial bus. This makes detection of frequency-dependent faults more difficult when using single-ended IEEE 1149.1 test approaches. In addition, AC-coupling blocks DC 1149.1 test patterns, rendering it completely ineffective.

A unique feature of some newer multichannel high-speed SerDes products is an at-speed built-in self-test (BIST) mode that can test the high-speed signal path. This test mode is sufficient for evaluating interconnects at the system operating speed (not at the slower test speeds), and it also works in an AC-coupled environment. At-speed BIST can be initiated and verified using the IEEE 1149.1 architecture.

For at-speed BIST to work, a serial bus must have a driver and receiver from the same vendor, a setup that is not always practical to implement. Although simple buffers and switches have become more popular for improving signal integrity of FPGA I/O or for boosting signals, at-speed BIST isn't efficient in these relatively simple products because it adds cost and complexity. It is also a synchronous approach, but simple buffer and switch components don't otherwise require a clock. A standardized pseudo-random pattern is still required to use at-speed BIST across products from different vendors. At-speed BIST produces pass/fail test results without any diagnostic capability.

Enter IEEE 1149.6

To address the issues associated with testing AC-coupled interconnects, the IEEE developed IEEE 1149.6. This standardized test approach makes interoperability of 1149.6 features across vendors and across differential interface technologies possible. Its simple implementation makes it practical for testing even basic PHY devices. Furthermore, software tools can provide comprehensive diagnostic capability for the targeted fault dictionary.

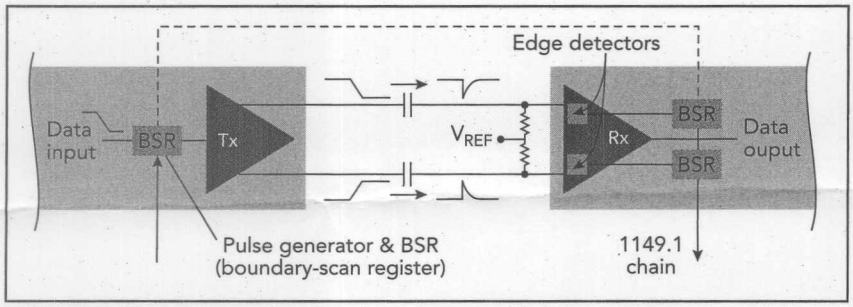

FIGURE 2. Capacitors pass pulses from a transmitter to a receiver

An IEEE 1149.6-compliant driver must incorporate the circuitry to generate high-speed pulses, initiated on IEEE 1149.1-delivered instructions (**Figure 2**). These high-speed pulses will pass through the coupling capacitors, and an 1149.6-compliant receiver must detect the pulse edges and provide a pass/fail indication through the IEEE 1149.1 interface.

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IEEE 1149.6 adds two opcodes, EXTEST_PULSE and EXTEST_TRAIN, that you can use to activate test modes. EXTEST_PULSE initiates a single pulse. EXTEST_TRAIN sends a series of pulses from the driver to the receiver, and it lets you charge the transmission line when you don't use an external reference. You must charge the line so the differential pair can operate within the normal common-mode range of the receiver.

Design challenges

To maximize IEEE 1149.6's effectiveness, the circuitry in a compliant device must not impact the device's mission mode (normal operation), especially the basic parameters of the individual signaling standards. Some minor impact to the receiver input structure such as a slight increase in output delay or added leakage or jitter might occur. The additional circuitry needed to support 1149.6 is manageable—providing the circuit designer is aware of the potential impact (Ref. 2, 3).

A second challenge comes in designing a methodology that will detect all possible faults in the high-speed interconnect. Although IEEE 1149.6 is intended as a universal solution for differential signaling, the implementation that works best in one termination scheme may not be the best approach for all termination schemes and all faults. There are a wide variety of differential interface technologies, and each requires a unique implementation because each has a unique fault dictionary. The various implementations of termination schemes and receiver fail-safe circuitry also add to the complexity of the fault dictionary. The best approach to address this challenge requires collaboration between the ATPG software vendor, the chip designer, and the board designer. T&MW

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